

U. S. Appln. No. 09/768,904

Amendment After Final dated November 12, 2003

Reply to Office Action dated September 10, 2003

Page 2

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:
 - (a) field oxide layer disposed on a semiconductor substrate and within a contact region;
 - (b) a metal plug contact disposed within [[a]] said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and
 - (c) a metal connected to said metal plug contact.
2. (Original) The device as claimed in claim 1, wherein said semiconducting device comprises integrated circuits.
3. (Original) The device as claimed in claim 1, wherein said field oxide layer further comprises silicon oxide.
4. (Original) The device as claimed in claim 2, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.
5. (Currently Amended) A method for preventing and/or thwarting reverse engineering, comprising steps of:
 - (a) providing a field oxide layer disposed on a semiconductor substrate and within a contact region;
 - (b) providing a metal plug contact disposed within [[a]] said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and
 - (c) connecting a metal to said metal plug contact.

U. S. Appln. No. 09/768,904

Amendment After Final dated November 12, 2003

Reply to Office Action dated September 10, 2003

Page 3

6. (Original) The method as claimed in claim 5, wherein said semiconducting device comprises integrated circuits.

7. (Original) The method as claimed in claim 5, wherein said field oxide layer further comprises silicon oxide.

8. (Original) The method as claimed in claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

9. (previously presented) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

- (a) field oxide layer disposed on a semiconductor substrate;
- (b) a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and
- (c) a metal connected to said metal plug contact.

10. (Original) The device as claimed in claim 9, wherein said semiconducting device comprises integrated circuits.

11. (Original) The device as claimed in claim 9, wherein said field oxide layer further comprises silicon oxide.

12. (Original) The device as claimed in claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

13. (previously presented) A method for preventing and/or thwarting reverse engineering, comprising steps of.

- (a) providing a field oxide layer disposed on a semiconductor substrate;
- (b) providing a metal plug contact disposed outside a contact region and above said field oxide layer, wherein said metal plug contact is electrically isolated from said contact region; and
- (c) connecting a metal to said metal plug contact.

U. S. Appln. No. 09/768,904

Amendment After Final dated November 12, 2003

Reply to Office Action dated September 10, 2003

Page 4

14. (Original) The method as claimed in claim 13, wherein said semiconducting device comprises integrated circuits.

15. (Original) The method as claimed in claim 13, wherein said field oxide layer further comprises silicon oxide.

16. (Original) The method as claimed in claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

17. (previously presented) The device as claimed in claim 1, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

18. (previously presented) The method as claimed in claim 5, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

19. (previously presented) The device as claimed in claim 9, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

20. (previously presented) The method as claimed in claim 13, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

21. (Canceled)

22. (Canceled)

23. (previously presented) The device of claim 9, wherein said metal plug contact contacts said field oxide layer.

24. (previously presented) The method of claim 13, wherein said metal plug contact contacts said field oxide layer.